

	Type	L #	Hits	Search Text	DBs
1	BRS	L1	10	prefetch\$3 adj loop	USPA T
2	BRS	L2	982	(prefetch\$3) and branch adj predict\$3	USPA T
3	BRS	L3	982	(prefetch\$3) and (branch adj predict\$3)	USPA T
4	BRS	L4	573	(prefetch\$3) same (branch adj predict\$3)	USPA T
5	BRS	L5	465	(prefetch\$3) with (branch adj predict\$3)	USPA T
6	BRS	L6	121	(prefetch\$3) with (branch adj predict\$3) and (external adj memory)	USPA T
7	BRS	L7	5	((prefetch\$3) with (branch adj predict\$3)) same (external adj memory)	USPA T
8	BRS	L8	195	SDRAM near5 fast\$3	USPA T
9	BRS	L9	137	SDRAM near3 fast\$3	USPA T
10	BRS	L10	34	direct adj map\$3 adj instruction adj cache	USPA T
11	BRS	L11	0	prefetch\$3 with (0request adj arbiter)	USPA T
12	BRS	L12	6	prefetch\$3 with (request adj arbiter)	USPA T
13	BRS	L13	38	prefetch\$3 with arbiter	USPA T
14	BRS	L14	2	960519.ap.	USPA T
15	BRS	L15	376	tagawa.in.	USPA T
16	BRS	L16	0	tagawa.in. and debug.clm. and (circuit near3 emulator)	USPA T
17	BRS	L17	12	debug.clm. and (circuit near3 emulator).clm.	USPA T
18	BRS	L18	22	debug.clm. and (circuit near3 emulator).clm.	USPA T; US-P GPUB

	Type	L #	Hits	Search Text	DBs
19	BRS	L19	2	tagawa.in. and debug.clm. and (circuit near3 emulator).clm.	USPA T; US-P GPUB
20	BRS	L21	645	712/205-207.ccls.	USPA T
21	BRS	L22	1254	712/233-241.ccls.	USPA T